



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,645	12/04/2003	Paul Metzgen	ALT-291	8459
36981	7590	02/09/2005	EXAMINER	
FISH & NEAVE IP GROUP ROPES & GRAY LLP 1251 AVENUE OF THE AMERICAS FL C3 NEW YORK, NY 10020-1105			TAN, VIBOL	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary

Application No.

10/728,645

Applicant(s)

METZGEN ET AL.

Examiner

Vibol Tan

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2003.
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) ☒ Claim(s) 1-33, 47 and 48 is/are allowed.
 6) ☒ Claim(s) 34 and 37-46 is/are rejected.
 7) ☒ Claim(s) 35 and 36 is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____.
 5) ☐ Notice of Informal Patent Application (PTO-152)
 6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 34, 37-46 and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal et al. (U. S. PAT. 6,097,212).

In claim 34, Agrawal et al. teaches all claimed features in Fig. 11B, a multiplexer circuit comprising: L look-up tables (LUT'a', LUT'b'); a plurality of data inputs (In0-In3), each of said data inputs being connected to one of said L look-up tables; and C control inputs (select0 for LUT'a', Select0 for LUT'b', and Select1); wherein: $C = L + 1$ ($3=2+1$).

In claim 37, Agrawal et al. further teaches a programmable device (mentioned throughout Agrawal reference) comprises multiplexer circuit of claim 34.

In claim 38, Agrawal et al. further teaches a digital processing system comprising: processing circuitry (processing means; col. 54, line 44); a memory (memory means; col. 2, line 21) coupled to said processing circuitry (inherent); and a programmable logic device as defined in claim 37 coupled to the processing circuitry and the memory (inherent).

In claim 39, Agrawal et al. further teaches a printed circuit board (col. 5, line 4) on which is mounted a programmable logic device as defined in claim 37.

In claim 40, Agrawal et al. further teaches the printed circuit board defined in claim further comprising: memory circuitry mounted on the printed circuit board and coupled to the programmable logic device (inherent, that what pcb is used for mounting electronic devices such as memory, microprocessor, PLD etc...)

Claims 41-46 are rejected in the same manner as claims 37-40.

In claim 49, Agrawal et al. teaches all claimed features in Fig. 11B, a method for encoding control inputs of a multiplexer (1100B) having C said control inputs (select0 for LUT'a', Select0 for LUT'b', and Select1), said method comprising: at any one time, asserting only one of a subset of all (activating Select0 for both LUT) but a reserved one of said C control inputs (Select1 not activated) in a first logic state, with each other of said subset of said control inputs being in a second logic state different from said first logic state (the first logic state not the same as the second logic state); and applying a

Art Unit: 2819

signal (either low or high) to said reserved one of said C control inputs (Select1) in either said first logic state or said second logic state.

4. Claims 35 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 1-33 and 47-48 appear to comprise allowable subject matters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VIBOL TAN
PRIMARY EXAMINER